

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **05-206412**

(43)Date of publication of application : **13.08.1993**

(51)Int.Cl.

H01L 27/115

G11C 16/02

G11C 16/04

(21)Application number : **04-307798**

(71)Applicant : **SEMICONDUCTOR
ENERGY LAB CO LTD**

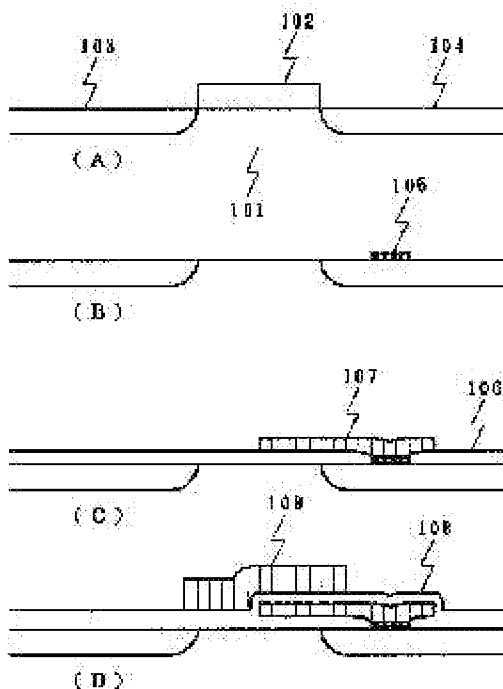
(22)Date of filing : **21.10.1992**

(72)Inventor : **YAMAZAKI SHUNPEI
TAKEMURA YASUHIKO**

(30)Priority

Priority number : **03309914** Priority date : **29.10.1991** Priority country : **JP**

(54) SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURE



(57)Abstract:

PURPOSE: To provide a high-reliability semiconductor memory device wherein the number of rewrite operations is enhanced by a method wherein an insulating material whose interatomic bond is strong is used limitedly for a route in which electric charges are moved to a floating gate.

CONSTITUTION: A mask material 102, a source region 203 and a drain region 204 are formed selectively on a semiconductor substrate 101; a thin film 105 composed of silicon nitride, oxynitride silicon, silicon carbide or aluminum oxide is formed selectively in one part on the drain. The surface of the substrate is oxidized. A silicon oxide film 106 which contains 0.01 to 5 atomic % of chlorine or fluorine is formed to be thicker than the insulator 105 by using an ion irradiation technique. A floating gate 107 is formed on it. Lastly, a silicon oxide film 108 is

formed in the same manner as in conventional cases; then, a control gate 109 is formed.

Thereby, it is possible to realize a semiconductor memory which increases the reliability of an EEPROM and which increases the number of write and erasure operations.